DEVELOPMENT OF FPGA MICROBLAZE PROCESSOR AND GSM BASED HEART RATE MONITORING SYSTEM

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Abstract

The research work presented in this paper shows the development of a system capable of sending the real-time heart rate of a patient under observation on a cellular phone in the form of Short Message Services (SMS). The system makes it possible to keep in touch with a physician; especially, when the patient's heart functioning shows some kind of diseases like arrhythmia. By observing any of the unexpected heart rates on the cellular phone itself, the consultant may ask the patient to do some essential exercises so as to avoid any life threatening situation. The Universal Asynchronous Receiver / Transmitter (UART) Soft IP Core was designed using Xilinx MicroBlaze Processor to send necessary Attention (AT) commands and drive the Global System for Mobile Communication GSM Module. Xilinx Field Programmable Gate Array (FPGA) Spartan 3E device was selected for implementation of the MicroBlaze processor Soft IP Core.

Keywords: FPGA; GSM; Heart Rate; MicroBlaze Processor; SMS; UART

1. Introduction

The present paper is an outcome of a research work in which an embedded system was developed for Heart Rates monitoring using the Field Programmable Gate Array (FPGA) and Global System for Mobile Communication (GSM) interface. The prototype developed here sends heart rate of the patient under observation through the FPGA and GSM module. Usually, when patient is under stress and there is no facility available to monitor the heart status, the patient has to be admitted in the hospital. Most of the time it is observed that, when patient is in the hospital and under observation of the physician; his heart rates shown by measuring instrument may show the normal results. The bottleneck arises when such a patient is under stress and there is no provision of monitoring him by a physician or a doctor, so that he would be asked to undergo through some exercises and hence avoid heart attack or any abnormal behaviour of the heart.

A prototype of a simple and non-invasive system to remotely monitor the real-time heart rate of patients or individuals based on phonocardiography, the study of heart sounds has been developed. The system consists of five modules. The first module, namely the front-end module is used to acquire and capture heart sound signals. Signal transmission and reception is done wirelessly using the FM transmitter & receiver module, this is reported by (Lee, Y.M, Moghavvemi, M., 2002). The system is based on microcontroller PIC16F877 and heart rates are displayed on Visual Basic (VB) based computer.

However the present prototype developed in this research work display the heart rates on a mobile cellular phone in the form of Short Message Services (SMS). The moment when patient wishes to communicate the physician then he is just to press the push button available on the system. The message "Heart Beats/m= ...." with heart rate would be sent to the doctor's mobile phone located anywhere over the globe. Looking at these values the consultant may inform to do some exercise and avoid any life threatening situation of the patient.

The Xilinx Spartan 3E FPGA was deployed to drive the GSM SIM 300 module and send pre-loaded message with recently captured values of heart rates. The reconfigurable device was hardwired using FPGA based 'MicroBlaze' processor; working as Universal Asynchronous Receiver / Transmitter (UART). As given in (MicroBlaze Processor Reference Guide, 2012), the MicroBlaze soft core processor is highly configurable, allowing select to its specific set of features required by user design. The fixed feature set of the processor includes: Thirty-two 32-bit general purpose registers, 32-bit instruction word with three operands and two addressing modes, 32-bit address bus and Single issue pipeline. In addition to these fixed features, the MicroBlaze processor is parameterized to allow selective enabling of additional functionality.

The eight bit values associated with the heart rates were input to the general purpose input output lines of the MicroBlaze processor; configured in the FPGA. A bit-stream (.bit) file for the development of MicroBlaze hardware-platform was initially generated, following to which an Executable and Linkable (.elf) was imported from Xilinx tool: Software Development Kit (SDK). Combining these two files, a final .bit file was generated in Xilinx ISE Project Navigator tool and hardwired into the FPGA board ROM. The GSM SIM300 module was interfaced with the UART implemented in the MicroBlaze to send SMS. Prior to interfacing of the GSM module with UART port of the FPGA board, a hyper terminal screen test of the processor was carried out.

2. Designing MicroBlaze Processor based UART Using Xilinx Core Generator

The CORE Generator System is a design tool that delivers parameterized cores optimized for Xilinx FPGAs. It provides a catalogue of ready-made functions ranging in complexity from simple arithmetic operators such as adders, accumulators, and multipliers, to system-level building blocks such as filters, transforms, FIFOs, and memories, which is given in (Reference guide, 2011).

A MicroBlaze MCS embedded processor was designed using Xilinx ISE Design flow. The Core-Generator was used to design the processor. The processor core was located in Embedded Processing menu of the Architecture Wizard Intellectual Proprietary (IP) Cores. Such a system development was targeted for Spartan 3E FPGA board (Nexys2); developed by Digilent Inc. It consists of the on-board clock source producing 50 MHz clock signal. Therefore, the input clock frequency for the MicroBlaze processor was configured to the same figure. The memory size for the processor was set to 16KB. To input the digital data pertaining to the heart rates, a GPI port of the processor was set to accept an 8 bit value. While sending the binary towards the GSM module, it was also necessary to monitor what values it sends serially, that's why an output was also taken from the processor output and displayed on the Light Emitting Diodes (LEDs) available on the board. For that the MicroBlaze GPO port was set to the same number of outputs to that of GPI port. The UART port of the processor was programmed to send ASCII data elements serially at the baud rate of the order of 9600. The UART Receiver and Transmitter were enabled.

The Figure 1 illustrates the darkened input output lines of the MicroBlaze processor; indicating the ports that are being utilized in this soft IP core development. The 'Generate' button on the wizard shown in Figure1 generates the Xilinx core with .xco and it was shown in the hierarchy of the main project. A top level entity in Very High Speed Integrated Circuit Hardware Description Language (VHDL) was developed using the VHDL instantiation template; generated by the Core Generator itself. The following code lines of source code developed for final top level module are as shown below.
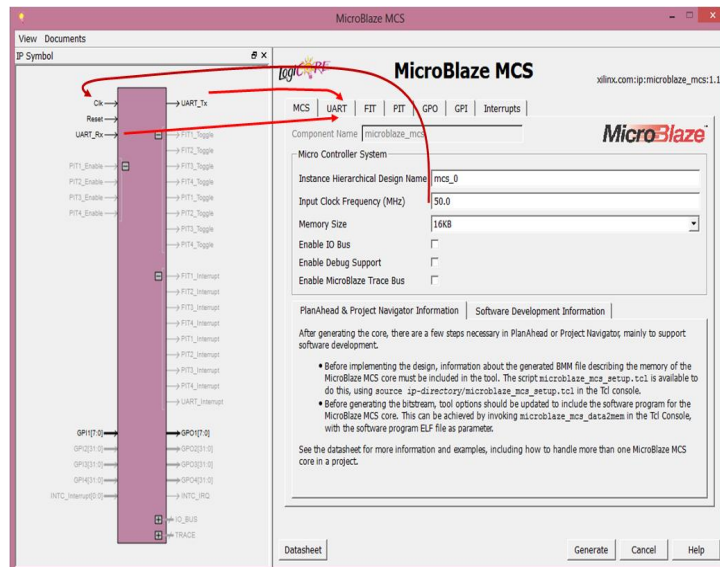
Figure 1: Xilinx MicroBlaze MCS Processor Configured for 50 MHz input clock, 9600 Baud Rate for UART and 8 bit GPI/GPO
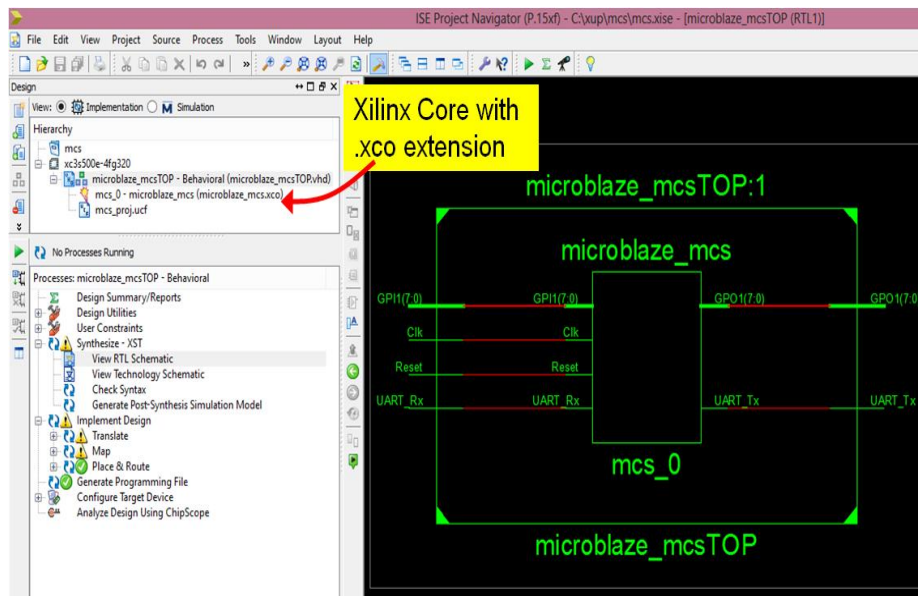

Figure 2: Register Transfer Level (RTL) Synthesis View of the Top Level Entity with Xilinx Design Flow Hierarchy

entity microblaze_mcsTOP is
PORT (
    Clk : IN STD_LOGIC;
    Reset : IN STD_LOGIC;
    UART_Rx : IN STD_LOGIC;
    UART_Tx : OUT STD_LOGIC;
    GPO1 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);

```
   GPI1 : IN STD_LOGIC_VECTOR(7 DOWNTO 0)
 );
end microblaze_mcsTOP;
architecture Behavioral of microblaze_mcsTOP is
COMPONENT microblaze_mcs
 PORT (
  Clk : IN STD_LOGIC;
  Reset : IN STD_LOGIC;
  UART_Rx : IN STD_LOGIC;
  UART_Tx : OUT STD_LOGIC;
  GPO1 : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
  GPI1 : IN STD_LOGIC_VECTOR(7 DOWNTO 0)
 );
END COMPONENT;
begin
mcs_0 : microblaze_mcs
 PORT MAP (
  Clk => Clk,
  Reset => Reset,
  UART_Rx => UART_Rx,
  UART_Tx => UART_Tx,
  GPO1 => GPO1,
  GPI1 => GPI1
 );
```

The VHDL lines of source code show that there is a top level entity 'microblaze_mcsTOP' having I/O port same to that of the 'microblaze_mcs'; a component generated by core generator. In the architecture body of the top level entity this component was instantiated with instance name 'mcs_0'. This default name ('mcs_0') was given by the core generator itself; during the process of core generation. Failing to give this instance name the *.xco* core would not be successfully instantiated in the top level module.
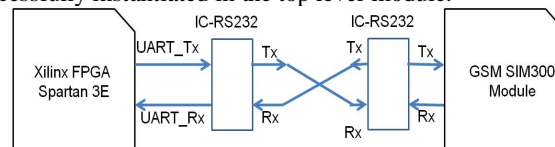

Figure 3: AT Interfacing of FPGA MicroBlaze Processor based UART with GSM SIM300 Module

3. Synthesis Result of the Top Level Module Structured with the Xilinx Core

As given in (Wikipedia Document, 2013), Synthesis is a process of compiling the high level or abstract level design (e.g. VHDL) and converting into the implementation platform such as Application Specific Integrated Circuit (ASIC) or Field Programmable Gate Array. The synthesis result of the top level module 'microblaze_mcsTOP' in the form of Register Transfer Level (RTL) view is shown in Figure 2. It depicts the Design window of Xilinx ISE Design flow, it shows the hierarchy level of the Soft IP Core and the user constraint file (.ucf) developed to interconnect necessary FPGA I/O pads with the top level entity. The Figure 2 shows 'microblaze_mcs' component interconnected with the 'microblaze_mcsTOP' VHDL entity. It depicts an 8 bit input vector named as GPI(7:0), a global clock 'Clk' and 'Reset' etc. To perform UART operation, and receiving the serial bit stream, another input port designated as 'UART_Rx' is also shown in Figure 2. At the other side of the module, an output port 'UART_Tx' is shown, that transmits the serial bits towards the GSM module. The 8 lines of top level module were given to the LEDs available on the Nexys2 Spartan 3E board. The Figure 2 illustrates such output vector designated as GPO(7:0).
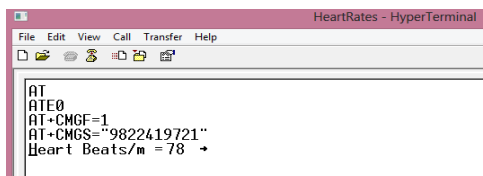
4. Verification of FPGA MicroBlaze Processor Based UART with GSM Module

The GSM Modem can accept any GSM network operator SIM card and act just like a mobile phone with its own unique phone number. Advantage of using the modem is that it can be used with its RS232 port to communicate and develop embedded applications. Applications like SMS Control, data transfer, remote control and logging can be developed easily. The modem can either be connected to PC serial port directly or to any microcontroller. It can be used to send and receive SMS or make/receive voice calls. The details of the Attention (AT) Commands useful to perform different tasks from this module are also given in (Datasheet, 2013).

The Figure 3 illustrates the detailed interfacing of the GSM SIM300 module with FPGA implemented MicroBlaze processor; working as UART. The FPGA based UART communicates with the GSM UART port using cross connection of the receiver and transmitter lines. That means the 'UART_Tx' (transmitter line) from FPGA UART was connected with the 'Rx' (receiver) terminal. Similarly 'UART_Rx' from FPGA was connected to the 'Tx' of GSM module. These all interconnections were done through voltage converter ICs RS232; embedded on both the modules. The necessary AT commands were sent from FPGA MicroBlaze Processor based UART to drive the GSM SIM300 module; prior to which the same commands being generated from FPGA were tested on the Hyper Terminal of the Personal Computer. Figure 4 illustrates a hyper terminal screen-shot taken at the time of testing FPGA UART.

The 8 bit FPGA input port was stimulated with a signal pertaining to the heart beats of 78 beats per minute. After generating necessary AT commands as shown in Figure 4, the receiver's mobile number was also displayed. The displayed message would be sent to the receiving mobile phone only when the ASCII code corresponding to the 'Ctrl+Z' was received by GSM module. For that purpose the 'Ctrl+Z' associated code was sent to the hyper terminal for testing purpose of FPGA based UART following to the character string "Heart Beats/m = 78".

The Nexys2 FPGA board has a UART port. The Xilinx device xc3s500e-4fg320 was mounted on the board developed by Digilent Inc. The details of other interfacing and features provided on the board are given in (Reference manual, 2011).

Figure 4: Hyper Terminal window and AT Commands necessary for GSM SIM300 Module Driving

5. Conclusion

The research paper uses Xilinx Core Generator to design MicroBlaze processor based UART, which is able to drive a GSM module by sending AT commands. The 8 bit input for this Soft IP Core implemented in Xilinx FPGA Spartan 3E is given which is associated with the Heart Rates of a patient under observation of a physician. The FPGA sends AT commands to the GSM SIM300 module, therefore consequently the module sends an SMS (to the doctor) indicating the status of a patient pertaining to the heart beats per minute.

References:

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