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Leakage Power Minimization in ST-SRAM Cell Using Adaptive Reverse Body Bias Technique

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Abstract

Nowadays, we all are using battery operated devices and the devices require extremely low power to maximize the lifetime of the battery. Maximum devices are storing their data in memory. With downscaling of CMOS process, low power operation is the main area of importance in memory design. Power reduction can be achieved by many techniques. Here, in this paper, the main focus and analysis is Schmitt Trigger based SRAM (ST-SRAM) cell and use of adaptive reverse body bias technique to minimize leakage power. The total circuit simulation has been done using 180nm Technology in Cadence. Static Noise Margin is calculated here to check the read stability of the circuit. The adaptive reverse body bias technique used here increases the threshold voltage and reduces the leakage power.

Keywords: BTBT, CMOS, DIBL, GIDL, SNM

1. Introduction

As VLSI in developing rapidly, which emerge in the form of advanced and sophisticated devices in which there is a decreased the device geometrics, increased the density as well as the complexity of the circuit. According to this the stuff which is being used in our day to day life is coming in the form of the smaller unit having multitasking characteristics. But there are also some drawbacks in this i.e., it consumes more power and generates more heat. Hence, the device which consumes more power is more susceptible to runtime error as well as less reliable. So, keeping all these issues in mind now a day's designers are work to design such a device which mainly consumes less power at all levels of the design. So memory is an important aspect to work on in the development of some new designs. SRAM is a usually considered by the designers as a valuable concept because as it is volatile in nature and with high speed and faster in performance as compared to DRAM. But SRAM consumes more power so this is the main concept of motivation i.e., the design of SRAM using an advanced technique to reduce the power and leakage minimization as well as increasing the stability of the circuit(Ray, Mandal, & Patro, 2016).

The rest part of paper composed of discussion on related work which is done in the previous issue in section 2, the discussion about all basic concepts of SRAM, its leakage power and the current components in section 3, the discussion on the working of the proposed design for leakage power reduction. Section 4 includes the simulated results of the work. Section 5 is about the conclusions and finally, the paper end with references.

2. Related Works and Important Parameters

There are several designs have been proposed previously based on voltage and timing specifications. By describing the basic concepts of 6T SRAM, in a similar manner, the description is done on the designs from 4T to 10T. In Figure1, the architecture of the previously published SRAM bit cell has been shown (Kulkarni &

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Roy, 2012). In this design of the 4T SRAM cell has been discussed where the circuit is a load less configuration, PMOS devices act as the access transistors (Noda, Matsui, Takeda, & Nakamura, 2001).

In case of the 5T SRAM, it is based on the asymmetric cross-coupled inverter with a single bit line (Jain, 2012). The bit line has been pre-charged with separate voltages. Though there been used separate voltages for pre-charge, still then in the intermediate cases of voltages a dc-dc converter in required due which the requirement of additional design margin would be needed for the PVT corners which would violate its applicability. Then comes the 6T design, in which two cross-coupled inverters are connected back to back having two NMOS as the access transistors. Write operation is done by the modulation of the virtual VDD and virtual VSS.

In case of the 7T, it has separate read port and the write operation (Suzuki, Yamauchi, Yamagami, Satomi, & Akamatsu, 2008). In case of the single-ended design, the write operation has been done either due to asymmetrical inverter characteristics or differential VSS/VCC bias. And during the read operation, the extra transistor turned off. When 7T design operates in the differential mode the feedback path between the two inverters gets cut-off during the write operation.

In 8T design, resembles 6T SRAM cell only there are the extra transistors connected to the later design for the separate read and write operation.

Then for 9T SRAM design, the bit-cell is designed with differential read which is considered to be a disturb-free operation. And in 10T design, single-ended resembles the single-ended 8T designs read and write operation.

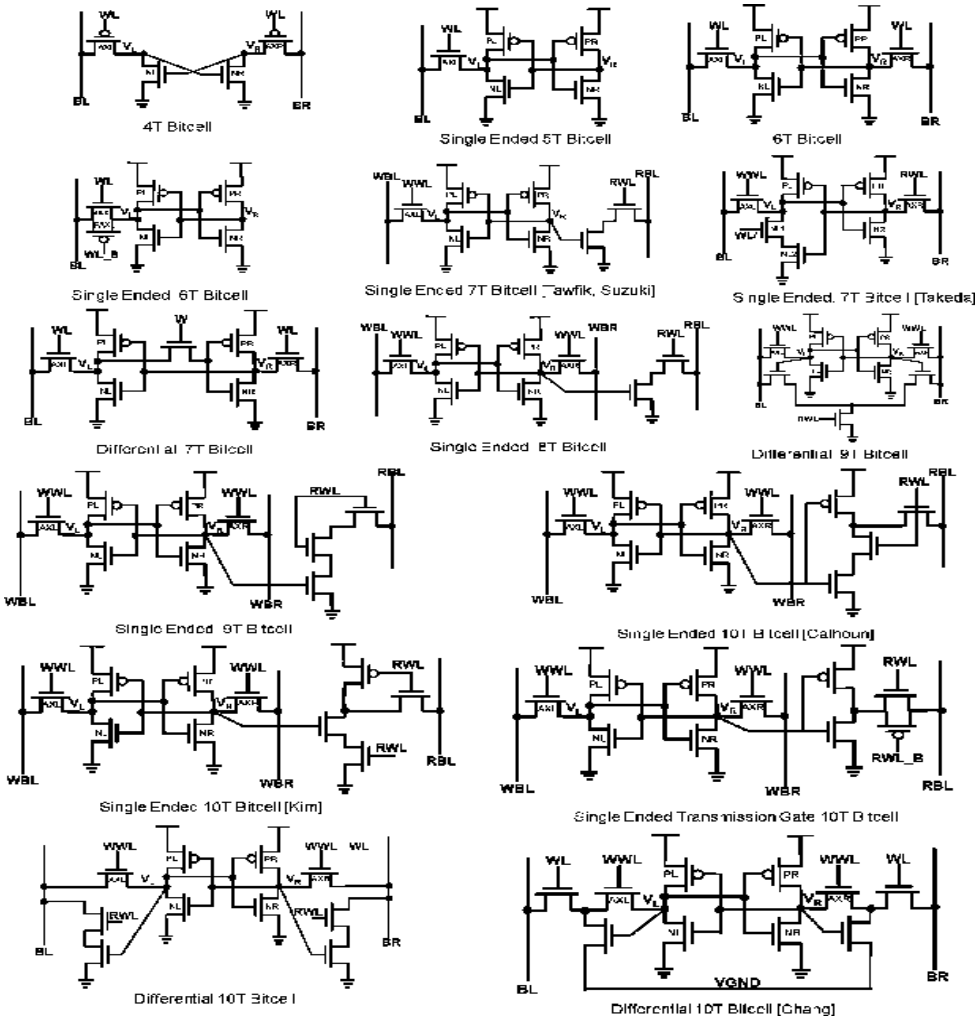

Figure1: Previously Published SRAM Bit Cell configuration

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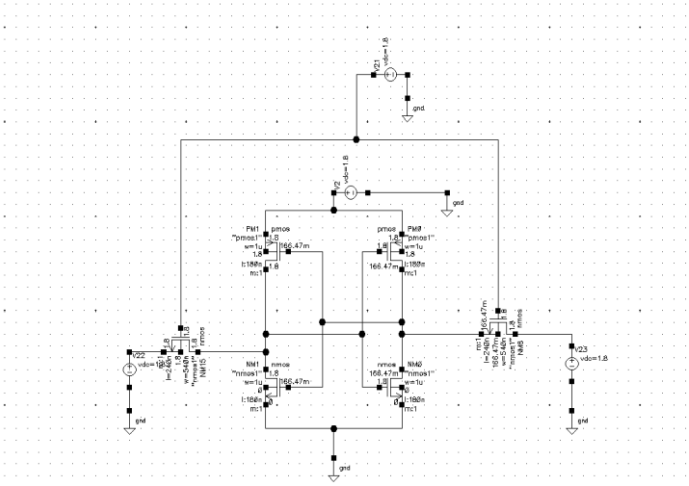

Figure 2: The Conventional circuit of the 6T SRAM cell

2.1 Basics of SRAM (Static Random Access Memory)

The SRAM cell consists of a static latch, containing two cross-coupled inverters. It does not need any *periodic refreshing* to maintain the data, endowed with that there is sufficient voltage power supply for the cell. Figure 2, shows the simulation circuit of conventional 6T SRAM Cell where the two cross-coupled inverters are connected back-to-back (two PULL UP transistors and two PULL DOWN transistors).There are two access transistors. When the word-line (WL) is enabled, the access transistors are turned on and connect the storage nodes to bit- lines. In other words, they allow access to the cell for reading and write operations, performing as bidirectional transmission gates.

The 6T SRAM cell performs three operations -
1) READ operation
2) WRITE Operation
3) STANDBY operation

READ operation

During a read operation, the bit-lines are pre-charged to high voltage and voltage of high value is applied to word-line. During a read operation, a sense amplifier is connected to detect the state of the cell. Throughout the read operation, the cell ratio should be suitably large to make sure that a read interruption does not take place.

WRITE operation

The bit-lines are driven to complementary voltage levels via a write driver and then the word-line is selected. To avoid write failure the cell gamma ratio should be satisfactorily large. Gamma ratio is the ratio of the strength of the pass-gate transistor to that of the pull-up transistor. All the bit-lines are pre-charged to the VDD at the end of the write operation and get prepared for next write or read operation.

STANDBY operation

When the world-line is not connected to the cell and the two pass transistors are disconnected from the bit-lines the SRAM cell is said to be in standby mode. In this operation, two cross-coupled inverters will keep on to support each other as long as they are linked to the supply (Kim & Kim, 2009).

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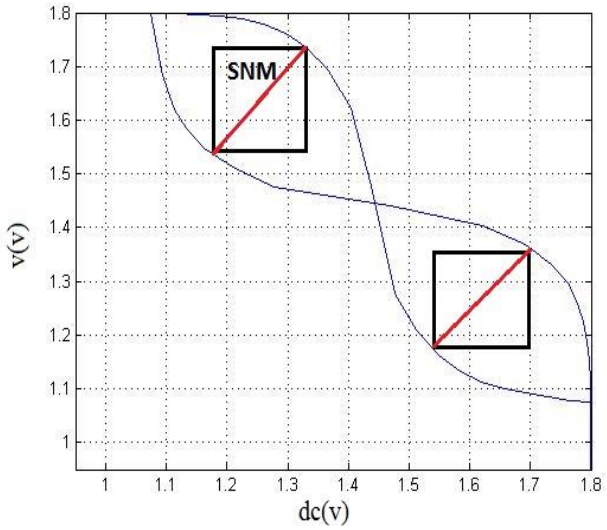

Figure 3: Static Noise Margin (SNM) for the Read operation of 6T SRAM cell

2.2 Static Noise Margin (SNM)

At a storage node, the highest passable DC noise voltage is known as SNM. A read disturbance does not occur for a good SNM (Tomar, Singh, & Akashe, 2011). It is measured by the length of the diagonal of the biggest square that can fit inside the butterfly curves.

SNM calculation

We have done the SNM calculation by this way with respect to above butterfly curve: SNM = 'Maximum length between the corner of the square'. Maximum length between the corner of the square = Maximum lengths of diagonal of Square / Square Root of 2. So, SNM = Maximum length of diagonal of square / Square Root of 2 (Chen, 2003; Kulkarni & Roy, 2012).

2.3 Leakage Current Components in CMOS

In Figure 4, basically, it consists of six leakage components. They are, $\mathbf{I_{GATE(GB)}}$ and $\mathbf{I_{GATE(DG)}}$ are the gate-to-bulk and drain-to-gate oxide tunnelling currents; $\mathbf{I_{PT}}$ is channel Punch-through current $\mathbf{I_{SUB}}$ is the sub-threshold current; $\mathbf{I_{GIDL}}$ is the gate induced drain leakage; $\mathbf{I_{BTBT(DB)}}$ and $\mathbf{I_{BTBT(SB)}}$ are the band-to-band tunnelling currents of the drain-to-bulk and source-to-drain junctions respectively due Junction leakage; and $\mathbf{I_{HC}}$ is the gate current due to hot carrier effect (Xiao, Liu, & Sun, 2011) . The gate leakage, BTBT current, and sub-threshold current are the dominating components in the total leakage. So, when V_{DS} of the cut-off transistors get reduced across the reverse-biased substrate-drain PN junction then other leakage components are considered to be negligible (Jeon, Kim, & Choi, 2010; Sharma & Soni, 2010).

Total Leakage current

The I_{OFF} is the leakage current when a transistor is in OFF state (when V_{GS}=0V for an NMOS device). Hence as per the discussion

$$\mathbf{I_{OFF} = I_{REV} + I_{GIDL} + I_{SUB}} \quad (1)$$

When $V_{DB} = V_{DD,}$ the $I_{REV,}$ and I_{GIDL} increases in their magnitude. Among the three components of I_{OFF} (total leakage current); I_{SUB} is clearly the dominant component. Hence the main target is now to work on $I_{SUB,}$ so that leakage power can get reduced i.e., by decreasing the sub-threshold leakage currents in circuits that are in active or standby state (Fallah & Pedram, 2005).

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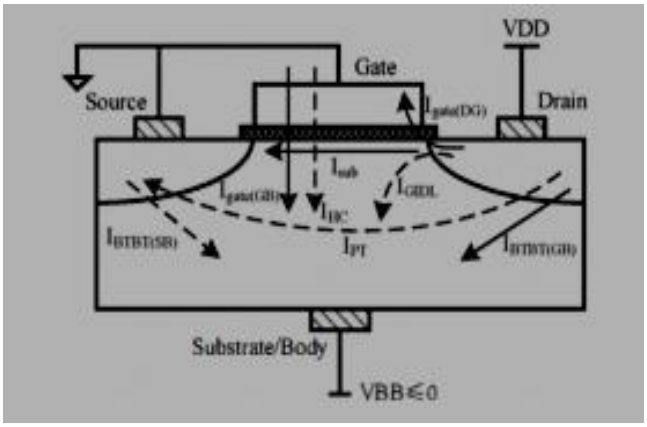

Figure 4: Leakage mechanism due to short-channel effect

2.4 Body Bias Control and Scaling of Power Supply

The Reverse Body Bias (RBB) technique is the appreciable method to reduce the leakage current[5]. With the help RBB the threshold voltage can get increased when the transistors are in the standby mode. By reverse biasing a transistor increases its threshold voltage and it can be done during a standby mode of operation, by applying a strong negative bias to the NMOS bulk via a charge pump and connecting the PMOS bulks (N wells) to the V_{DD} rail. But when the reverse body biasing (RBB) is applied to the PMOS transistors by raising the N-well voltages, a triple-well technology, which may not always be available.

3. Proposed Design

In the Figure5, where the 6T SRAM along with Schmitt Trigger is connected to the peripheral circuits, which includes three different circuits: 1) Leakage monitoring circuit 2) current comparator 3) body bias regulator circuit. The output generated from the body bias regulator is again fed back to the current difference generator circuit. The loop goes on till an optimal value is generated as V_{BODY}. This V_{BODY} will be provided to the target circuit i.e., 6T SRAM cell as an input. The Optimal value of the V_{BODY} will increase the V_{TH} of the transistor in SRAM and the leakage power will get reduced as the circuit operates at a high threshold.

3.1 Leakage Monitoring Circuit

The leakage monitoring circuit is shown in Figure 6, has current mirror circuit and a current differential amplifier circuit which will produce the two different current that is I_{SUB} and I_{BTBT}. There are two cluster circuits connected to the drain end of the current mirror so that the current will get replicated.

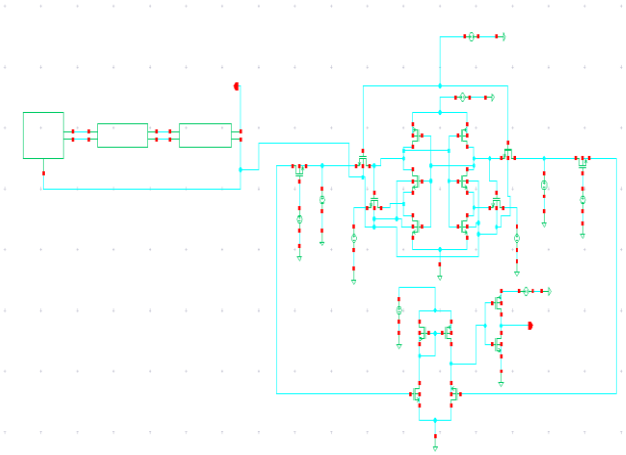

Figure 5: Schematic of the 6T SRAM cell along with Schmitt Trigger and Adaptive Reverse Body Bias Technique

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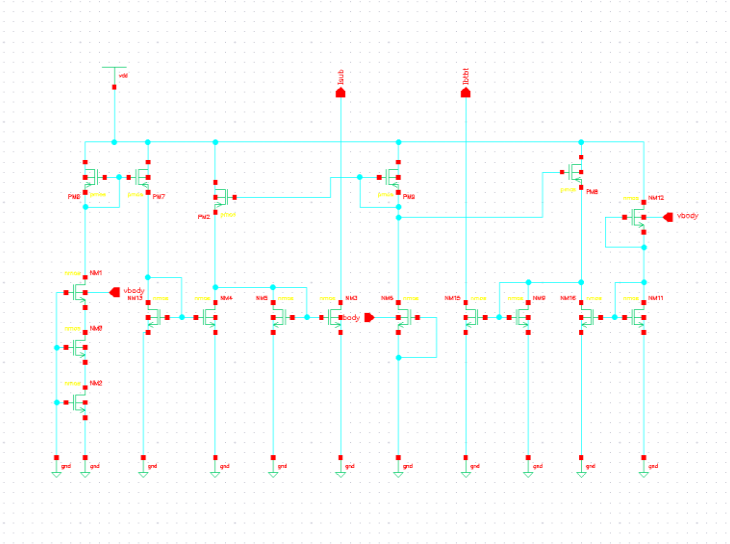

Figure 6: Schematic of the Leakage Monitoring circuit

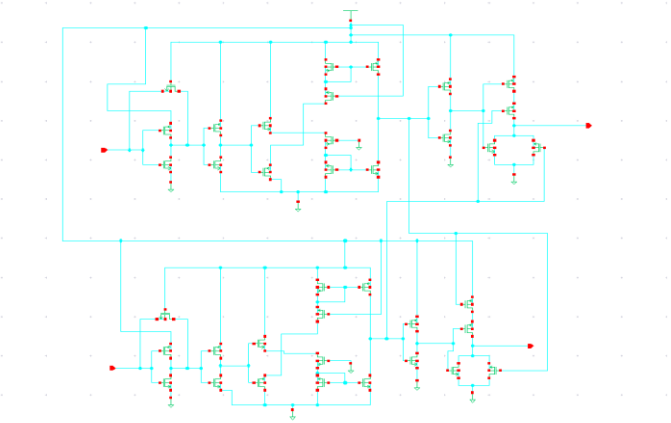

Figure 7: Schematic of the comparator circuit

3.2 Current Comparator Circuit

The current comparator circuit as shown in Figure 7 is getting its input from the current difference generator circuit which is preceding to the respective circuit. As the comparator circuit work as a class AB amplifier, so two different outputs are generated as UP and DOWN signal through four different logic gates. These outputs will be fed as inputs to the successive circuit, which is the charge pump circuit along with its output stage.

3.3 Charge Pump Circuit

The charge pump circuit gets input from the comparator as UP and DOWN signal. As the capacitor connected to it gets charged and discharged it produces output in the form of two different voltages at its output stage.
The whole design has to satisfy three conditions: 1) $I_1 < I_2$, UP=0 & DOWN =1, V_{BODY} decreases to reduce the total leakage. 2) $I_1 > I_2$, UP=1 & DOWN = 0, output of V_{BODY} regulator increases. 3) $I_1 = I_2$, $\Delta I_1 = 0 = \Delta I_2$, then an optimal value of the body bias found and that is to be maintained. Finally, the optimal value of V_{BODY} will be maintained and supplied as input to 6T SRAM cell which is the target circuit to minimize the leakage by calculating it from leakage current which is taken from the off state transistors.

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$$P_{LEAKAGE} = I_{LEAKAGE} * V_{DD} \quad (2)$$

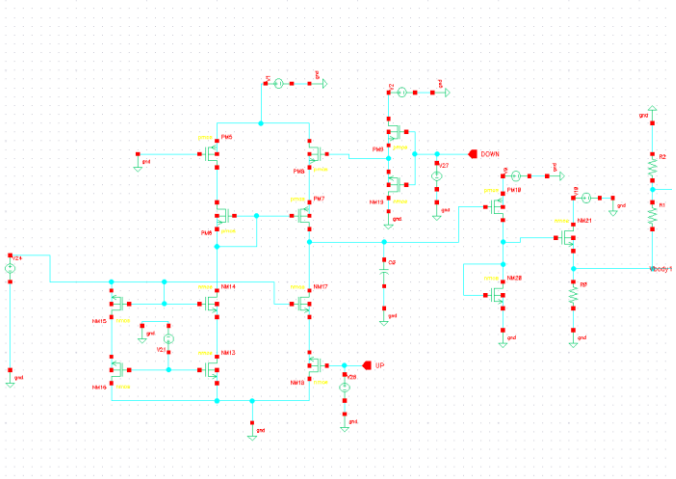

Figure 8: Schematic of the Charge Pump Circuit

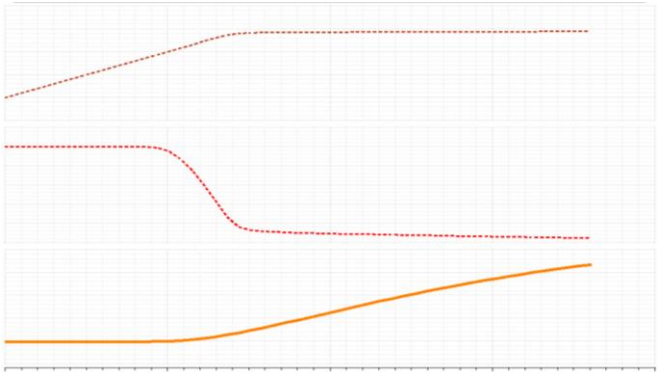

Figure 9: Simulated Output and Power Consumption Waveform of the ST-SRAM cell with Adaptive Reverse Body Bias Circuit

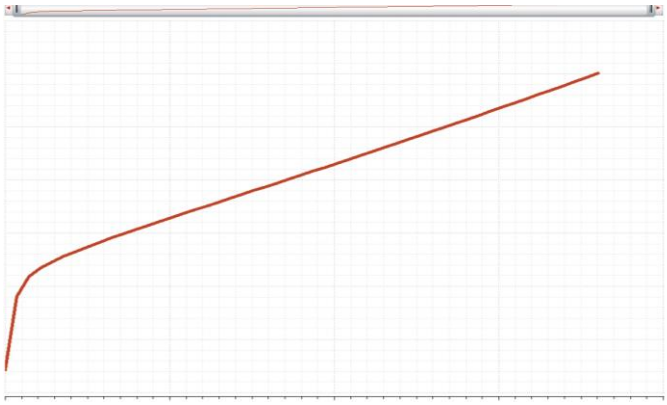

Figure 10: Output Waveform of Leakage Current of the ST-SRAM cell with Adaptive Reverse Body Bias Circuit

4. Simulated Output and Results

Figure 9 and Figure 10 show the simulated output waveform of power consumption and leakage current. From Table-1, it shows in 6T SRAM cell with ST and ARBB, the leakage power consumption gets reduced 96.44% than 6T SRAM cell. The SNM improves 5.6% than 6T SRAM cell, which indicates that the proposed SRAM cell is more stable than the 6T SRAM cell.

Table 1: Result Discussion of Leakage Power & SNM in 180nm Technology

Sl. No.	SRAM Cell	Leakage Power (in Watt)	SNM
1	6T SRAM	534.4E-9	463.23 mV
2	6T SRAM with ST	39.28E-12	416.07 mV
3	6T SRAM with ST & ARBB	15.01E-12	491.44 mV

5. Conclusion

This paper gives a summary that as the leakage power is an important aspect and it plays a dominant role in the total power of the design. Therefore, more attention has to be paid to the standby leakage power. The leakage can also be reduced if we do constant field scaling i.e., by reducing the supply, the threshold increases but it remains fixed at a certain value and beyond it, we can increase just by providing it a reverse body bias. But again there is a problem to increase the threshold to which value, hence to get an optimal condition the Adaptive Body Bias is a recommendable technique which after following a feedback loop and satisfying certain condition will provide an optimal value as body voltage to the target circuit transistors. So, in this manner, the threshold increases and leakage reduces without any violation to the performance of the target circuit.

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A Brief Author Biography

Dr. Kananbala Ray has completed Ph.D in Low Power SRAM design from KIIT Deemed to be university. She is presently working as Assistant Professor in School of Electronics Engineering, KIIT Deemed to be University, Bhubaneswar, Odisha, India. Her area of research includes low power digital circuit design.

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