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Performance Evaluation of Various Discrete Cosine Transforms

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Abstract

Digital signal processing (DSP) algorithms exhibit an increasing need for the efficient implementation of complex arithmetic operations. Coordinate transformations of complex valued phasors and the computation of trigonometric functions is sort of naturally involved with modern DSP algorithms. One of the most computationally high algorithms called the Discrete Cosine Transform. Discrete cosine transform (DCT) is widely used transform in image and signal processing and it has a strong property which is energy compaction. Most of the signal information is concentrated in a few low-frequency components of the DCT. It's a real transform with better computational efficiency and it does not introduce discontinuity while imposing periodicity in the time signal. Many DCT algorithms were proposed in order to achieve high speed DCT and low power consumption. CORDIC algorithm can be widely used in Software Defined Radio, wireless communications and medical imaging applications. These are heavily dependent on signal processing. The algorithm is very much hardware efficient because it performs combination of shift-add operations and omits the dependence on multipliers. This article discusses the CORDIC algorithm and various DCT performances in the Digital Signal Processing.

Keywords: Discrete Cosine Transform **(**DCT**)**, 1D DCT, 2D DCT, Distributed Arithmetic DCT, CO-ordinate Rotation Digital Computer (CORDIC).

Introduction

The rapid growth of digital imaging and signal applications, including teleconferencing, desktop publishing, multimedia, high-definition television (HDTV), error detection and correction in transmission as well as data compression has increased the need for effective and standardized image and signal compression techniques. The emerging standards are JPEG, for compression of still images and MPEG for compression of motion video. All of these standards are employs a basic technique known as the discrete cosine transform (DCT). D**iscrete Cosine Transform (DCT)** expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. An efficient hardware implementation of various DCT enhances the accuracy of reconstruction of the original data. It will decrease chip area by decreasing the number of computations, so that the power consumption is also reduced. **1D Discrete Cosine Transform (1D DCT)** is useful in one-dimensional signals processing such as speech waveforms. It has most often been used in 2D DCT, by employing the row-column decomposition. The Discrete Cosine Transform of a one dimensional sequence of length N is defined as ,

$$F(u) = \alpha(u) \Sigma f(x) \cos [pi(2x+1)u/2N]; \text{ for } u=0,1,2\ldots N-1$$

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α(u) is defined as
α(u)= sqrt(1/N) for u=0
sqrt(2/N) for u≠0

2D Discrete Cosine Transform (2D DCT) algorithms are the most widely used transform in image compression. Row-Column 2D DCT implementation performs better, when the optimized 1D DCT block along rows and columns are used. The hardware is also required to achieve the high-speed processing in real-time applications. The 2D DCT is an extension of the 1D case and it is given by,

$$C(u,v) = \frac{1}{4}\alpha(u)\alpha(v)\sum_{x=0}^{N-1}\sum_{y=0}^{N-1} f(x,y)\frac{\cos(2x+1)u\pi}{2N}\frac{\cos(2y+1)v\pi}{2N}$$

For u, v=0,1,2,…..N-1.

Distributed Arithmetic (DA) will perform the arithmetic operation such as addition, multiplication and it can be used in signal processing. Distributed Arithmetic used for computing the Discrete Cosine Transform and its inverse. It is basically bit serial computational operation and that forms an inner product of pair vector in single direct step. DCT architecture based on distributed arithmetic which is a multiplier less architecture. It is widely used in VLSI realization because of improvements in area, power consumption and speed.

CO-ordinate **R**otation **DI**gital **C**omputer (**CORDIC)** is an efficient, fast, simple and powerful algorithm which is used in many Digital Signal Processing applications. It uses a unique computing technique which is mainly suitable for solving the trigonometric relationships involved in plane co-ordinate rotation and conversion from rectangular to polar form. It is normally used when no hardware multiplier is available such e.g., simple microcontrollers and FPGAs as the only operations it requires are addition, subtraction, bit shift and table lookup.This article discusses the CORDIC algorithm and various DCT performances in the Digital image and Signal Processing.

Methods and Materials

Discrete Cosine Transform

M Thiruveni and M Deivakani (2012) designed an analog VLSI architecture for Discrete Cosine Transform. Signal Processing is an area that deals with analysis and operation of signals. It can be classified as Analog and Digital Signal processing. For the digital signal processing, the real time analog signals are reborn to digital, processed and return back to analog before given to globe. One of the important tools of digital signal processing algorithms is Discrete Cosine Transform (DCT). It is novel approach of analog CMOS implementation technique for Digital Signal Processing (DSP) algorithms. Analog DCT consists of three major blocks

- Multiplier cell
- Adder cell
- Sample and Hold

The sample is increased with DCT coefficient in opamp SHA amplifier and added using opamp adder. The circuits are simulated by using Tanner spice.

Integer DCTs (IntDCTs) for lossless-to-lossy image coding transform required to redesign the devices. Lossless image coding is used in high-end hardware for medical images, remote sensing, image archiving and satellite communications. Taizo Suzuki and Masaaki Ikehara (2010) designed an Integer DCT Based on Direct-Lifting of DCT-IDCT for Lossless-to-Lossy Image Coding. A discrete cosine transform (DCT) can be easily implemented in software and hardware for the JPEG and MPEG formats. Lossy image coding is used in low-end hardware for digital camera and Internet contents. Lossless image coding provides information integrity that is maintained throughout the entire encoding

and decoding process. IntDCT is implemented by direct-lifting of DCT and inverse DCT (IDCT). This integer DCTs is designed by using lifting-based filter banks (LBFBs), and it have been projected for lossless-to-lossy image coding.

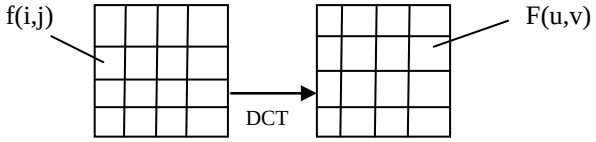

Fig.1 DCT

Jridi M and Alfalou A, (2010) presented a new design of low-power and high-speed Discrete Cosine Transform (DCT) for image compression is to be implemented on Field Programmable Gate Arrays (FPGAs). The compression method used to converts the image to be compressed in many lines of 8 pixels and then applies our optimized DCT algorithm for compression. The DCT optimization is relies on the hardware simplification of the multipliers used to compute the DCT coefficients. By using constant multipliers based on Canonical Signed Digit (CSD) encoding, the number of subtracters, adders and registers are minimized. A new technique based on Common Sub expression Elimination (CSE) is analyzed to decrease the number of required subtracters and adders operators by using FPGA Spartan3E device.

Chiper D F et al.., (2007) proposed unified design framework for prime-length forward and inverse discrete cosine transforms with a high throughput. This method facilitates trade-off between the throughput and hardware cost or power consumption, and it is well suited for low-power applications. It is based on the derivation of new economical heartbeat algorithms. The algorithms have the constant core structure for both transforms, and the core structure has two circular correlations, which is different from other similar computational structures, it has the same length. It can be computed in parallel and mapped on the same linear heartbeat array with channels having a low I/O bandwidth requirement and their numbers are independent of the transform length N. It can be efficiently enforced on the same VLSI chip.

1D Discrete Cosine Transform

Do Kyoung Shin et al.., (2014) designed a new methodology of detection text regions from video sequences, without previous data such as font, color, size of characters. By analyzing the characteristics of text regions in video sequences, text regions embrace each horizontal and vertical edges are found at the same time, whereas background regions do not. The adaptive thresholding technique used to detect text regions accurately and the user object regions detected through 1D-DCT.

Priya S and Kumar J V (2012) proposed comprised design of Distributed Arithmetic (DA) based VLSI architecture of DCT for reducing the facility consumption. The circuit is intended with low power consumption techniques by exploitation of low power logical components that is depends upon the system clock. This system consists of two modules where the first module is basically the design of 1D Discrete cosine transform and another one is 1D Discrete Cosine Transform using distributed architecture. The simulation is performed by using Modelsim simulator and power consumption can be calculated by using ALTERA power estimation tool.

New Distributed Arithmetic (NEDA) has been applied to the 1-D DCT to produce a low power and high throughput architecture. NEDA can be applied into the even-odd decomposition matrices of the 8×8 forward and inverse DCT. Chidanandan A et al.., (2006) designed Area-Efficient NEDA Architecture for the 1-D DCT/IDCT. In this approach, the number of adders required for the adder array for the forward DCT and the inverse DCT is lesser than the NEDA is applied directly to the 8×8 DCT and IDCT matrices. It may also reduce the number of adder stages.

Min Jiang et al.., (2004) designed 1D-DCT processor with parallel pipelined VLSI architecture for MPEG visual and audio applications. This processor is based on the distributed arithmetic to obtain high computations efficiency. The

simulation with EDA software is employed. The pipelined parallel architecture can be obtained an efficient compromise between hardware cost and computing speed for real-time MPEG-related applications. One primary advantage of the DCT over the DFT is that only involves in real multiplications, which reduces the total number of required multiplications.

2D Discrete Cosine Transform

Madanayake R et al., (2012) proposed an algebraic integer (AI)-based time-multiplexed row-parallel architecture and two final reconstruction step (FRS) algorithms for the implementation of bivariate AI encoded 2-D discrete cosine transform (DCT). FRS uses two approaches based on Expansion factor scaling and Optimized Dempster–Macleod multipliers. This architecture is directly realizes an error-free 2-D DCT without using FRSs between row–column transforms and it leading to an 8×8 2-D DCT that is entirely free of quantization errors in AI basis. It can be realized and verified on field-programmable gate arrays chip.

D.Preethi, A.M Vijaya Prakash (2012) proposed architecture in which DCT multipliers are replaced by using adders and shifters. The low power approaches like Canonic signed digit representation for constant coefficients and a sub-expression elimination methodology is used. The 2D DCT is performed on 8x8 image matrix using two 1D DCT blocks and a transposition block. As same as DCT, the IDCT is additionally implemented using the Lo.effler algorithm. Verilog HDL is used to implement the design. XILINX is used for the simulation of the design. CADENCE RTL compiler is used to synthesize and obtain the power and area of the design. MATLAB is employed because the support tool to get the input constituent values of the image. Since no multipliers used in the design and very low power can be obtained.

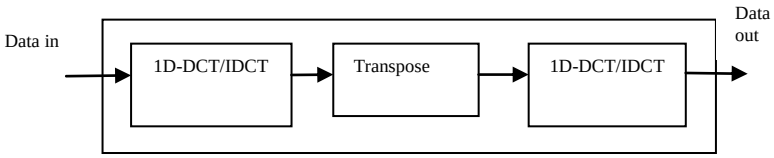

Fig.2 Architecture of 2-D DCT

The bi-dimensional for Multimedia applications particularly used for the cryptography and decipherment of normal image and video formats. In graphic compression algorithms, the bi-dimensional Discrete Cosine Transformation (2D-DCT) is commonly used frequency transformation. Several hardware implementations, adopting disparate algorithms are planned for Field Programmable Gate Arrays (FPGA). These designs concentrate either performance or an area. Antonino Tumeo et al.., (2007) designed a quick 2D DCT hardware accelerator for a FPGA-based SoC. This accelerator can makes use of a single seven stages 1D-DCT pipeline and it can be able to alternate computation for the even and odd coefficients in each cycle. In additionally, it uses special recollections to perform the transpose operations. Hardware takes 80 clock cycles at 107MHz to generate a complete 8x8 2D DCT, from the writing of the first input sample to the reading of the last result (including the overhead of the interface logic).

A 2D discrete cosine transform (2D DCT) has become a very popular transform in video compression and some other real-time applications. Pankaala M et al.., (2004) presented the Realization of an analog current-mode 2D discrete cosine transform. This DCT algorithm is used to achieve the high speed DCT and it involves multipliers for example Chen's algorithm has less regular architecture due to complex routing and requires large silicon area. The designed structure is faster than other and it has small power consumption and takes a small silicon area.

Distributed Arithmetic Discrete Cosine Transform

Akhter S, Karwal V and Jain R C (2013) proposed VHDL implementation of Odd Discrete Cosine Transform (ODCT-II) coefficient computation using independent update algorithm. By independent, ODCT coefficient computation of shifted data sequence doesn't require ODST coefficients of previous data. The running input file sequence is sampled using a rectangular window. The freelance update algorithm is used to compute the transform coefficients of the shifted sequence using Distributed Arithmetic (DA) approach. The design is synthesized mistreatment ISE 10.1 and enforced on Vertex four.

Rizk M R M and Ammar M (2007) presented an efficient algorithm for implementing the Discrete Cosine Transform (DCT) with Distributed Arithmetic (DA). The design is free of multipliers, computer storage and computer storage accumulators. Inner product of computational module has been proved mathematically, for require only additions. The numbers of additions are decreased by dividing the adder array matrix before exploiting the redundancy in it. It uses the recursive DCT algorithm, it requires less area than the conventional approaches and fifteen additions, four subtractions are needed to complete the calculations. Hardware implementation of the look is realized on Xilinx FPGA XC3S1000.

In the direct approach, large number of multiplications and additions are required to compute two-dimensional (2D) DCT. Multiplications are the most time-consuming operations in simple processor and it can be completely avoided in the VLSI architecture for real-time image compression. Yanling Chen et al., (2007) proposed an area efficient high performance VLSI architecture for DCT based on the distributed arithmetic. Minimum number of additions is used in the DCT by exploiting the timing property of the DCT transform based on the distributed arithmetic.

Shams A et al.., (2002) presented a new distributed arithmetic architecture (NEDA). It is a low power optimized architecture based on the distributed arithmetic paradigm. In addition to low power performance, it gives high speed and reduced coverage area. In NEDA, scalar product computational module has been proved, mathematically and it is need only additions. Moreover, minimum range of additives is employed by exploiting the redundancy within the adder array. Such properties have created a NEDA unit a basic computational module for prime performance DSP architectures. The 8×8 DCT NEDA-based architecture is analyzed and Savings exceeding 88% are achieved for the DCT implementation.

Coordinate Rotation Digital Computer

Prasannan N (2014) presented low-power co-ordinate rotation digital computer based reconfigurable discrete cosine transform architecture. All the computations in DCT aren't equally necessary in generating the frequency domain output. Number of computations is more vital for determining the output image quality while others play relatively less important roles. Thus the numbers of CORDIC iterations are often controlled by considering the importance of DCT coefficients. The necessary distinction within the DCT co-efficient the quantity of CORDIC iterations can be dynamically changed to reduce the power consumption. The CORDIC based 2D DCT architecture is simulated using Modelsim and it achieves power savings with improved image quality.

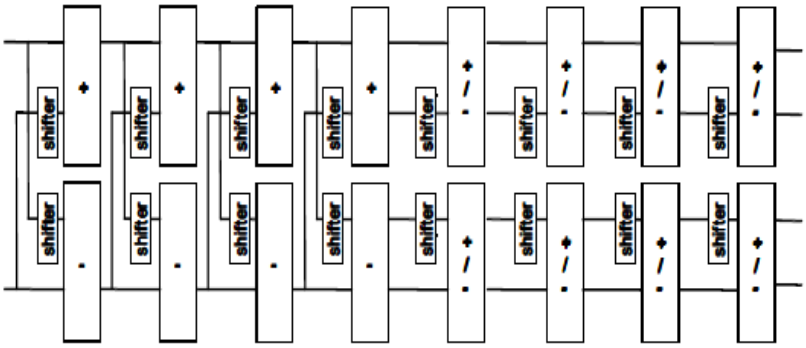

Fig.3 Basic CORDIC Architecture

Sang Yoon Park et al., (2012) designed the Fixed-Point Analysis and Parameter Selections of MSR-CORDIC with Applications to FFT Designs. Mixed-scaling-rotation (MSR) coordinate rotation digital computer (CORDIC) is an attractive approach to synthesizing complex rotators. The fixed-point error analysis of the FFT is presented when MSR-CORDIC is employed for the twiddle factor multiplier. The CORDIC algorithm is more hardware-friendly than the multiplication and accumulation (MAC) unit since it can be implemented by pipelined structures of sub modules using only shift and add operations. Modified CORDIC algorithms are used to improve the accuracy, latency and complexity of the computation.

The COordinate Rotate DIgital Computer (CORDIC) algorithm is a well known versatile approach and it is widely applied in today's SoCs but it is not restricted to digital communications. U Vishnoi et al., (2012) implemented CORDIC blocks in deep sub-micron CMOS technologies at very low area and energy costs. Optimizing Global Navigation Satellite System (GNSS) receivers reduce the hardware complexity. CORDIC accelerators can be used for digital baseband processing .The adders and shifters are play an important role in optimizing the CORDIC block, and they must be carefully optimized for energy efficiency and high area in the underlying technology. For this purpose carry-select adders and logarithmic shifters have been used. In this method area will be reduced and power consumption also reduced.

Huan Li Sch et al.., (2010) designed modified CORDIC algorithm and its implementation based on FPGA. In conventional CORDIC algorithm, a lookup table and multiplier are needed to achieve calculation of multiple transcendental functions and it will lead to hardware circuit complexity and lower operation speed. Modified CORDIC algorithm does not need the module of correction factor and the lookup table, and it used a simple shift and add-subtract to achieve the calculation of multiple transcendental function. This overcomes the shortcomings of traditional CORDIC algorithm and it can be implemented by FPGA program.

Results

M.Thiruveni and M.Deivakani(2012) concluded that analog architecture for DCT is better than digital DCT in terms of area and power. Round off noise is removed in the analog DCT. Taizo Suzuki, Masaaki Ikehara (2010) showed that IntDCT is better coding performance than the conventional methods in lossless-to-lossy image coding. A small side information block (SIB) which is validated by its application to lossless-to-lossy image coding. Jridi M, Alfalou A (2010) used Canonical Signed Digit (CSD) encoding to reduce the number of Arithmetic operations. It produce e less material complexity and a dynamic power saving. Chiper D F et al.., (2007) used systolic algorithms retain the benefits provided by VLSI implementations based on circular or cyclic convolution structures, and at the same time it has a simpler control structure, high speed and low complexity.

Do Kyoung Shin et al.., (2014) shown that the adaptive thresholding technique successfully detects text regions regardless of environmental conditions such as low contrast, complex texture, and various colors and sizes. Priya S and Kumar J V (2012) used low power consumption techniques by using low power logical elements. This technique reduces the glitches and unwanted delays produced in design. Chidanandan A et al.., (2006) concluded that the reduction results in power savings, without decreasing the throughput and in inverse DCT, the number of adder stages is reduced, resulting in faster decoding. Min Jiang et al., (2004) results shows that it provide low power and high computation efficiency.

Madanayake R et al., (2012) used FRS techniques and achieved complete elimination of quantization noise coupling between DCT coefficients. D Preethi, A M Vijaya Prakash (2012) proved lo.effler algorithm in 2D DCT provides very low power and low latency. Antonino Tumeo et al., (2007) concluded that the architecture provides optimal performance or area ratio with respect to several alternative designs and it reduces impact on occupation. Pankaala M et al.., (2004) shown that the accuracy requirements for converting either I- or P-frame differ and this reflects to the layout area of the structure and it consume less power.

Akhter S, Karwal V and Jain R C (2013) computed the transform coefficients of the shifted sequence using Distributed Arithmetic (DA) approach. It is more efficient for device utilization. Rizk M R M and Ammar M (2007) achieved high speed and the area is reduced by using recursive DCT algorithm. Yanling Chen et al.., (2007) analyzed 8 times 8 DCT architecture based on the DA and it reduce the area. Shams A et al.., (2002) showed 8×8 DCT NEDA-based architecture used to achieve high speed, low power and reduced area.

Prasannan N (2014) concluded that the reconfigurable CORDIC based DCT architecture can dynamically change the modes with power savings and it improves the image quality. Sang Yoon Park et al., (2012) shown that the number of adders and word-length are minimized when the SQNR of the FFT output is constrained. U Vishnoi et al., (2012) used deep sub-micron CMOS technologies at very low area and energy costs and it is attractive to be used as hardware accelerators for Application Specific Instruction Processors (ASIPs). Huan Li Sch et al.., (2010) results concluded that the modified CORDIC Algorithm is able to reduce hardware costs and improve operational performance.

Architecture	**Power Consumption in mW**
DCT	1.058 W
1D DCT	13.1 W
2D DCT	2.488
DA based DCT	5.78
CORDIC	0.184

Table- Power analysis of different architecture

The above comparison table shows the various architectures in terms of power consumption. Of these CORDIC algorithm in DCT seems to be the best by consuming less power than the other architectures.

Conclusion

This article illustrates the performance of various DCT and CORDIC algorithm in DSP applications to achieve high accuracy and low power. Commonly DCT and CORDIC algorithm are used in various real time applications such as teleconferencing, desktop publishing, multimedia, high-definition television (HDTV), communication systems, robotics

and 3-D graphics apart from general scientific, technical computation and biomedical applications etc. Thus in future it promotes a way for challenging applications in digital signal and image processing.

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