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REVIEW OF TWO DIMENSIONAL ANALYTICAL MODEL OF DUAL MATERIAL GATE TUNNEL FIELD EFFECT TRANSISTOR

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Abstract

In this paper, a new two dimensional (2D) analytical model of a Dual Material Gate tunnel field effect transistor (DMG TFET) is presented. The parabolic approximation technique is used to solve the 2-D Poisson equation with suitable boundary conditions. The simple and accurate analytical expressions for surface potential and electric field are derived. The electric field distribution can be used to calculate the tunneling generation rate and numerically extract tunneling current. The results show a significant improvement of on-current and reduction in short channel effects. Effectiveness of the proposed method has been confirmed by comparing the analytical results with the TCAD simulation results.

Keywords: Tunnel field effect transistor (TFET), Band to band Tunneling, Analytical model, Poisson Equation, Parabolic approximation, Surface potential

1. INTRODUCTION

As MOSFETs reach nanometer dimensions, power consumption becomes a major bottleneck for further scaling. The continued reduction of the MOSFET size is leading to an increased leakage current due to short channel effects, Such as Drain Induced Barrier Lowering (DIBL), and the power supply voltage cannot be reduced any further because of the subthreshold slope being limited to 60 mV/decade at room temperature. In this view, the exploration of alternative devices which possibly outperform the MOSFET at these nanometer dimensions is required. A promising alternative for the MOSFET, which does not suffer from these limitations, is the tunneling field-effect transistor (TFET). Throughout the rest of this paper the term TFET will not refer to any specific implementation form, but the TFET is defined as ”a semiconductor device in which the gate controls the source-drain current through modulation of Band-to-Band Tunneling (BTBT)”. Band-to-Band Tunneling is a process in which electrons tunnel from the valence band through the semiconductor band gap to the conduction band or vice versa. TFETs with a subthreshold slope lower than 60 mV/decade have already been demonstrated, and due to their built in tunnel barrier, Si TFETs are expected to maintain low off currents for channel lengths down to 10 nm.

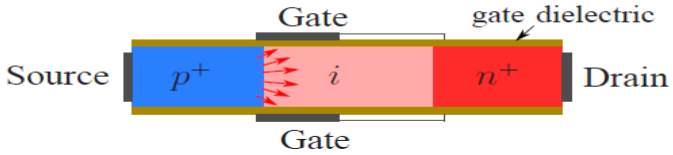

Fig.1. Double gate TFET with full (solid) and short (dashed) gate

An advantage of TFETs compared to other alternative device concepts is that their fabrication is compatible with standard CMOS processing since they can be implemented as a reverse biased gated PN diode. Moreover, compared to for example the I-MOS, TFETs do not rely on high energetic processes like impact ionization, which are known to be detrimental to reliability. Contrary to the MOSFET and the bipolar transistor, the TFET does not have a simple analytical model. This hampers a clear understanding of the TFET working principle. The gate lengths are scaled down to sub-100 nm and gate oxide thickness to below 3 nm, short-channel effects (SCEs) such as:

1) Increase in effective gate oxide thickness (EOT) due to polysilicon gate depletion;
2) Threshold voltage change due to boron penetration from p+ polysilicon gate into the channel region;
3) Degradation of device reliability due to gate leakage current (hot-electron effects); and
4) Reduced gate controllability due to drain-induced barrier lowering (DIBL) become predominant.

These SCEs need to be eliminated or minimized for proper device operation. To eliminate polysilicon depletion width effects and polysilicon dopant penetration, polysilicon gates need to be replaced by metal gates. The dual-material-gate (DMG) FET was proposed and fabricated, taking two different metal gates as gate electrode. DMG FET has two laterally contacting gate materials with different work functions to achieve threshold voltage modulation and improved carrier transport efficiency. Shur proposed a new field-effect transistor (FET) where the gate voltage swing (i.e., the difference between the gate voltage and the threshold voltage) is varied along the channel in such a way that the charge carriers are accelerated more rapidly and the average carrier velocity in the channel is increased. This can be achieved either by making the threshold voltage to be a function of position or by using a new device structure called split-gate FET (SG FET) If a more positive gate voltage is applied near the drain side than the electric field distribution along the channel is modified such that the electric field near the source becomes larger causing an increase in the gate transport efficiency. The realization of the SG FET structure is not a difficult task, but the fringing capacitance between two metal gates increases as the separation between them is reduced and degrades the device performance. However, this can be rectified if the separation between the two gates is made to be zero, but that leads to the conventional single gate structure.

2. RELATED WORK

FET structure, proposed by Long et al. [3] is that the dual-material gate (DMG) FET, employing "gate-material engineering" to improve both carrier transport efficiency and SCEs. The gate material with higher work function near the source end acts as the "control gate", while the gate material with lower work function near the drain end acts as the "screening gate" that prevents any changes in the drain bias to affect the channel region under the first gate. In the DMG MOSFET, two metals M1 and M2 of different work function are amalgamated together laterally. The work function of M1 is greater than M2 i.e. FM1 > FM2. Such a configuration introduces a step function in the potential along the channel such that the electric field distribution is enhanced at the source side to increase the carrier velocity while the drain potential change will be screened. Work function in M2 is chosen greater than M1 for a p-channel MOSFET and vice-versa for an n-channel MOSFET. Inspire of the several benefits offered by gate material engineering, the major issue of concern is the viability of fabrication.

Recently, Sarkar et al. [4] has emphasized the challenges and current status of the fabrication of DMG MOSFET. Recently, the multiple gate MOSFETs like Double-gate (DG) [5], triple gate [6],FINFET [7] and surrounding gate (SG) [8] MOSFETs has manifested themselves as the most popular candidate for nanoscale design for providing a better scalability option [9]. Excellent short channel affects (SCEs) immunity, high transconductance and near ideal subthreshold slope have been reported by many theoretical and experimental studies on this device [10].

A dual-material double-gate (DM-DG) SOI MOSFETs proposed by Reddy et al. [11] employs gate-material engineering to reduce SCEs significantly when compared to with the DG SOI MOSFET. To get further improvement against SCEs Tiwary et al. [12] proposed TM-DG MOSFET and also developed an analytical subthreshold model. It is inevitable that all variants of FinFETs will finally change to surrounding gate nanowire FETs, because of their best electrostatic gate-control, higher control of SCEs and larger channel area for the nanowire surface per unit area [13-15].

Yu et al. [16] reported an accurate 2-d analytical model of surrounding gate MOSFET using Bessel functions. On the other hand, surface- potential based model with moderate accuracy such as [17-19] uses the simple polynomial approximation of the potential profile to offer reduced computational burdens and is suitable for the circuit simulation and the device design as compared to Fourier series based approaches [20]. On the other hand, superposition technique based modeling approach was also reported [21], requiring a large computational burden. A computationally efficient modeling based on pseudo-2d approach using Gaussian box in circular coordinates was also proposed[22,23].

Recently Sharma et al. [24] reported a more accurate isomorphic polynomial potential distribution based modeling approach. However, in this study we have chosen parabolic potential based approach due to its simplicity and reduced computational complexity. To incorporate the advantage of the gate engineering techniques combined with the structural advantage of surrounding gate MOSFET, a novel device structure called Dual Material Surrounding Gate (DMSG) MOSFET is proposed [25].

Later, Chianget al. reported an analytical subthreshold model using superposition technique [26]. On the other hand, Wang et al. developed a model for triple material surrounding gate MOSFET using superposition method [27]. Another superposition based model was reported for cylindrical surrounding gate MOSFET [28]. Recently, parabolic potential approach based model of triple material surrounding gate MOSFET was also reported [19].

Arobinda Pal al.et, in this paper, an analytical subthreshold model has been developed to study the effect of gate engineering on surrounding gate MOSFET to reduce SCEs by modeling surface potential, Electric Field, threshold voltage and drain current. Moreover, the effect of radius downscaling on the device performance was observed has also been studied. The analytical modeling demonstrate that DMSG MOSFET structure exhibits significantly enhanced performance in terms of threshold voltage roll-off and DIBL makes it a potential candidate for future generation n-MOSFET based circuits. The results are validated with numerical 2-D device simulation.

The aim of this work is, to study the potential benefits offered by the DMG TFET by using parabolic approximation technique for the first time, which is simple and accurate. The analytical model is developed using two dimensional solution of Poisson equation. This model is used to calculate the surface potential and electric field distribution in the device under the two metal gates and the drain current I_{DS} is derived from the electric field using Kane's model. The cross section view of a Dual Material Gate TFET is shown in Fig. 1. The source and drain is made of highly doped p-type and n-type regions respectively. The intermediate channel

region is made of a moderately doped n-type layer. Silicon-di-oxide (SiO_2) is used as the gate dielectric. If a positive gate voltage is applied, the transistor behaves as a n-TFET and a negative gate voltage is applied, the transistor behaves as a p-TFET. The device physical parameters are summarized in Table 1. Increasing the positive voltage on the gate narrows the energy barrier between the source and intrinsic region. Then electrons tunnel from the valence band of the p-doped source to the conduction band in the intrinsic body and then move toward the n-doped drain by drift diffusion. The bottom of the buried oxide (BOX) layer is grounded. The thickness of the BOX layer (t_{BOX}) is very small; hence the voltage drop across BOX region is negligible.

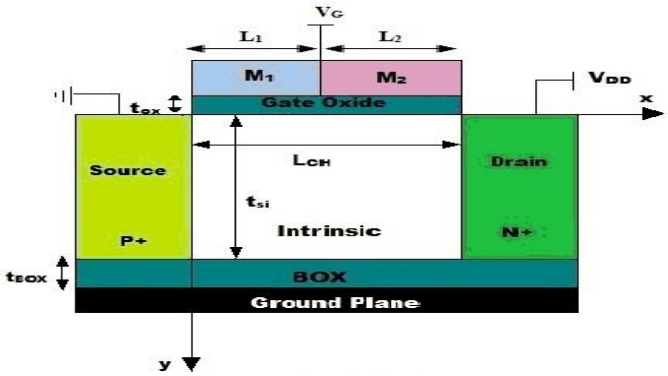

Fig.2. Schematic diagram of a DMG TFET

2.1 Surface potential

The potential distribution in the gate oxide region is distinguished by two dimensional Poisson's equation,

$$\frac{\partial^2 \phi(x,y)}{dx^2} = \frac{\partial^2 \phi(x,y)}{\partial y^2} = 0 \tag{1}$$

The potential profile in the vertical direction is assumed to be a second-order polynomial, i.e.,

$$\phi(x,y) = C_0(x) + C_1(x)y + C_2(x)y^2 \tag{2}$$

The boundary conditions in the channel region are:

(a) Electric flux at the front-oxide gate interface is continuous for DMG TFET, therefore

$$\frac{d\phi_1(x,y)}{dy} = \frac{\epsilon_{0x}}{\epsilon_{si}} \frac{\phi_{s1}(x) - \psi_{g1}}{t_{ox}} \text{ Under } M_1 \text{ at } y = 0 \tag{3}$$

$$\frac{d\phi_2(x,y)}{dx} = \frac{\epsilon_{0x}}{\epsilon_{si}} \frac{\phi_{s2}(x) - \psi_{g2}}{t_{ox}} \text{ Under } M_2 \text{ at } y = 0 \tag{4}$$

(b) Electric flux at the back gate-oxide and the back channel interface is continuous for both the material

$$\frac{d\phi_1(x,y)}{dx} = 0 \text{ Under } \mathrm{M_1} \text{ at } \mathrm{y = t_{si}} \tag{5}$$

$$\frac{d\phi_2(x,y)}{dx} = 0 \text{ Under } \mathrm{M_2} \text{at } \mathrm{y = t_{si}} \tag{6}$$

Where Vbi is the built in potential, Eg is Band gap energy, q is elementary charge, V_{GS} is Gate to Source voltage, V_{DS} is Drain to Source voltage, ε_{si} is relative permittivity of silicon and εox is relative permittivity of silicon dioxide.. The final coefficients of A, B, C and D can be expressed as

$$A = \frac{\left[\left(V_{bi} - \psi_{g1}\right)e^{\lambda(L1+L2)}\right] - \left[V_{bi} + V_{DS} - \psi_{g2}\right] + \left[\left(\psi_{g1} - \psi_{g2}\right)\cosh(\lambda_{L2})\right]}{e^{\lambda(L1-L2)} - e^{\lambda(L1+L2)}}$$

$$B = \frac{\left[V_{bi1} + V_{DS} - \psi_{g2}\right] - \left[\left(V_{bi} - \psi_{g1}\right)e^{\lambda(L1+L2)}\right] - \left[\left(\psi_{g1} - \psi_{g2}\right)\cosh(\lambda L_2)\right]}{e^{\lambda(L1-L2)} - e^{\lambda(L1+L2)}}$$

$$C = Ae^{(\lambda L1)} + \frac{\psi_{g1} - \psi_{g2}}{2}$$

$$D = Be^{-(\lambda L1)} + \frac{\psi_{g1} - \psi_{g2}}{2} \tag{7}$$

2.2 Electric field and Drain Current

The electric-field distribution along the channel length can be obtained by differentiating the surface potential. The mechanism of flow of current I_{DS} in DMG TFET is based on Band-to-Band Tunneling (BTBT) of electrons from the valance band of the source to the conduction band of the channel region. The tunneling generation rate (G) can be calculated using Kane's model. The total drain current is computed by integrating the band to band generation rate over the volume of the device.

$$I_{DS} = q\iint G dx dy \tag{8}$$

For the calculation of tunneling Generation rate (G), Kane's Model has been employed as,

$$G(E) = A\frac{|E|^2}{\sqrt{E_g}}\, e^{\left[-B\frac{E_g^{\frac{3}{2}}}{|E|}\right]} \tag{9}$$

$$|E| = \sqrt{E_x^2 + E_y^2} \tag{10}$$

3. CONCLUSION

In this work the DMG-TFET structure has been analyzed and their performance improvements over different parameters are discussed. The analytical model is based on two-dimensional Poisson's equation which is solved by using parabolic approximation. The analytical expressions of surface potential, lateral electric field and vertical electric field have been calculated. In this model, components of lateral electric field and vertical electric field can also be used to analytically calculate distribution of tunneling generation rate and numerically extract tunneling current. Based on the generation rate and electric fields, we obtained the I_{DS}-V_{GS} characteristics. From the presented results, it can be concluded that the DMG structure provides wide range of benefits to the TFET performance. The results clearly demonstrate the excellent immunity against SCE offered by the DMG structure while decreasing channel length.

REFERENCES

[1] ITRS, International Technology Roadmap for Semiconductors, 2009 (accessed26.05.11), http://www.itrs.net.
[2] X. Zhou, W. Long, A novel hetero-material gate (HMG) MOSFET for deepsubmicron ULSI technology, IEEE Trans. Elec. Dev. 45 (1998) 2546-2548.
[3] W. Long, H. Ou, J.-M. Kuo, K.K. Chin, Dual material gate (DMG) field effect transistor, IEEE Trans. Elec. Dev. 46 (1999) 865-870.
[4] Sarkar, A.K. Das, S. De, C.K. Sarkar, Effect of gate engineering in double-gate MOSFETs for analog/RF applications, Microelectron. J. 43 (2012) 873-882.
[5] A.A. Orouji, M. Jagadesh Kumar, A new symmetrical double gate nanoscale MOSFET with asymmetrical side gates for electrically induced source/drain, Microelectron. Eng. 83 (2006) 409-414.
[6] M.C. Lemme, T. Mollenhauer, W. Henschel, T. Wahlbrink, M. Baus, O. Winkler,R. Granzner, F. Schwierz, B. Spangenberg, H. Kurz, Sub-threshold behavior of triple-gate MOSFETs on SOI material sub-threshold behavior of triple-gate MOSFETs on SOI material, Solid State Electron. 48 (2004) 529-534.
[7] D. Hisamoto, L. Wen-Chin, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, K. Tsu-Jae, J. Bokor, H. Chenming, FinFET-a self-aligned double-gate MOSFET scalable to 20 nm, IEEE Trans. Electron. Dev. 47 (2000), 2320- 2325.
[8] B. Cousin, M. Reyboz, O. Rozeau, M.A. Jaud, T. Ernst, J. Jomaah, A unified shortchannel compact model for cylindrical surrounding-gate MOSFET, Solid State Electron. 56 (2011) 40-46.
[9] T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, K. Murase, Ultimate thin double-gate SOI MOSFETs, IEEE Trans. Elec. Dev. 50 (2003) 830-838.
[10] C.C. Tsai, Y.J. Lee, J.L. Wang, K.F. Wei, I.C. Lee, C.C. Chen, H.C. Cheng, Highperformance top and bottom double-gate low temperature poly-silicon thin film transistors fabricated by excimer laser crystallization, Solid State Electron.52 (2008) 365-371.
[11] G.V. Reddy, M.J. Kumar, A new dual-material double-gate (DMDG) nanoscale SOI MOSFETdTwo-dimensional analytical modeling and simulation, IEEE Trans. Nanotech. 4 (2005) 260-268.
[12] P.K. Tiwari, S. Dubey, M. Singh, S. Jit, A two-dimensional analytical model for threshold voltage of short channel triple-material double-gate metal-oxidesemiconductor field effect trans, J. Appl. Phys. 108 (2010), 074508-1-074508-8.
[13] H. Iwai, Roadmap for 22 nm and beyond, Microelectron. Eng. 86 (2009)1520-1528.
[14] V.M. Srivastava, K.S. Yadav, G. Singh, Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF Switch, Microelectron. J. 42 (2011) 112-1135.

[15] C. Li, Y. Zhuang, R. Han, G. Jin, J. Bao, Analytical threshold voltage model for cylindrical surrounding-gate MOSFET with electrically induced source/drain extensions, Microelectron. Reliab. 51 (2011) 2053-2058.
[16] B. Yu, Y. Yuan, J. Song, Y. Taur, A two-dimensional analytical solution for short-channel effects in nanowire MOSFETs, IEEE Trans. Electron. Dev. 56 (2009) 2357-2362.
[17] Kranti, S. Haldar, R.S. Gupta, Analytical model for threshold voltage and I-V characteristics of fully depleted short channel cylindrical/surrounding gate MOSFET, Microelectron. Eng. 56 (2001) 241-259.
[18] M.J. Kumar, A. Chaudhry, Two-dimensional analytical modeling of fully depleted dual-material gate (DMG) SOI MOSFET and evidence for diminished short-channel effects, IEEE Trans. Electron. Dev. 15 (2004) 569-574.
[19] P.S. Dhanaselvam, N.B. Balamurugan, Analytical approach of a nanoscale triple-material surrounding gate (TMSG) MOSFETs for reduced short-channel effects, Microelectron. J. 44 (2013) 400-404.
[20] G. Mei, G. Hu, S. Hu, J. Gu, R. Liu, T. Tang, Analytical model for subthreshold swing and threshold voltage of surrounding gate metal oxide semiconductor field effect transistors, Jpn. J. Appl. Phys. 50 (2011).
[21] J.H.K. Wang, S. Wu, T.K. Chiang, M.S. Lee, A new two- dimensional analytical threshold voltage model for short-channel triple material surrounding gate metal oxide semiconductor field effect transistors, Jpn. J. Appl. Phys. 51 (2012).
[22] Sarkar, S. De, A. Dey, C.K. Sarkar, 1/f noise and analogue performance study of short-channel cylindrical surrounding gate MOSFET using a new subthreshold analytical pseudo-two-dimensional model, IET Circuits Dev. Syst.6(2012) 28-34.
[23] Sarkar, S. De, A. Dey, C.K. Sarkar, A new analytical subthreshold model of SRG MOSFET with analogue performance investigation, Int. J. Electron. 99 (2) (2012) 267-283.
[24] D. Sharma, S.K. Vishvakarma, Precise analytical model for short channel cylindrical gate (CylG) gate-all-around (GAA) MOSFET, Solid State Electron. 86 (2013) 8-74.
[25] M.J. Kumar, A.A. Orouji, H. Dhakad, New dual-material SG nanoscale MOSFET: analytical threshold voltage model, IEEE Trans. Electron. Dev. 53 (4) (2006).
[26] T.K. Chiang, A new compact sub-threshold behavior model for dual-material surrounding gate (DMSG)MOSFET, Solid State Electron. 53 (2009) 490-496.
[27] J.H. KaiWang, S. Wu, T.K. Chiang, M.S. Lee, A new two-dimensional analytical threshold voltage model for short channel triple material surrounding-gate metal oxide semiconductor field effect transistors, Jpn. J. Appl. Phys. 51(2012) 054-301.
[28] Y. Pratap, P. Ghosh, S. Haldar, R.S. Gupta, M. Gupta, An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating

