V.Vijayabhasker *et al*, International Journal of Computer Science and Mobile Applications,
Vol.2 Issue. 12, December- 2014, pg. 53-57 **ISSN: 2321-8363**

STATIC TIMING ANALYSIS OF THE NON-GAUSSIAN VARIATION SOURCES FOR VLSI CIRCUITS

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Abstract: SSTA requires accurate statistical distribution models of non-Gaussian random variables of process parameters and timing variables. As CMOS technology scales down, process variation introduces significant uncertainty in power and performance to VLSI circuits and significantly affects their reliability. Although Static-Timing Analysis (STA) it is an excellent tool, but current trends in process scaling have imposed significant difficulties to STA. As one of the promising solutions, Statistical static timing analysis (SSTA) has become the frontier research topic in recent years in combating such variation effects. This paper will be focusing on two aspects of SSTA and its applications in VLSI designs: (1) Statistical timing modeling and analysis; and (2) Architectural implementations of the atomic operations (max and add). Experimental results have shown that our approach can provide 282 times speedup when compared to a conventional CPU implementation.

Index Terms- Statistical static timing analysis, CMOS, VLSI, non-Gaussian, process variations

I. INTRODUCTION

As the integrated circuit feature sizes approaches the wave length of optical lithography light source, process variation presents a serious challenge for the design of high performance circuit. [4]. Classical corner-based timing analysis methods produce timing predictions that are often too pessimistic and grossly conservative to be realistic. Instead, statistical static timing analysis (SSTA) that characterizes time variables as statistical random variables offers a much hope for more accurate and realistic timing prediction. Many existing SSTA algorithms assume that the statistical distributions of all process variables and timing variables can be approximated well by the normal distribution. While this assumption makes it easy to deduce the SSTA results, it is observed that such results often lack the accuracy that can be expected using the more laborious Monte Carlo simulation method. In particular, during timing analysis, non-linear operators such as the MAXIMUM (MAX) operation are often imposed on one or more timing variables.

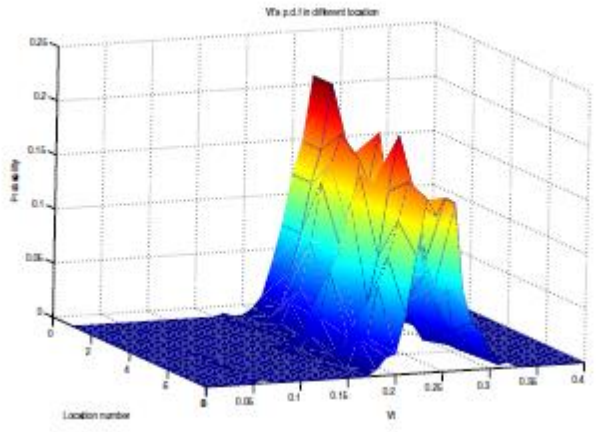

Figure 1. The threshold voltage distribution under 90 nm technology.

tributed, the output of the MAX operator of several Gaussian random variables is know to be non-Gaussian [1] [6]. To address this difficulty, recently, several non-Gaussian models have been proposed [7] [3] and [8] to model process parameters and timing variables. In [8] a quadratic Gaussian polynomial, $Y = aX2 + bX + c$, is proposed to model a non-Gaussian random variable. In this model, X is Gaussian random variable, and the parameters a, b, c can be derived using the first 3 moments of the random variable to be modeled. However, to ensure a, b, and c to be real numbers, the range of the skewness must be limited. Furthermore, higher order moments such as the *Kurtosis* can not be incorporated into this model. Since Kurtosis determines the peak of a distribution, failing to include it would produce inferior modeling results. For example, the empirical distribution of the threshold voltage of transistors of certain process is depicted in Figure 1. Note that the Kurtosis is different at different locations. Hence, it is crucial to model the Kurtosis accurately. To address these challenges, in this paper, we proposed two generalized non-Gaussian models that promise more accurate models of real-world process parameters and timing variables. The first model is a quadratic Gaussian polynomial model with complex valued coefficients. This way, a broader range of skewness can be modeled accurately. The second model is a higher order Gaussian polynomial model with the order being three or higher. This allows us to match higher order moments including Kurtosis with accurate representation.

II. SSTA

SSTA algorithms can be broadly categorized into path-based and block-based. The path based SSTA seeks to estimate timing statistically on selected critical paths. However, the task of selecting a subset of paths whose time constraints are statistically critical has a worst-case computation complexity that grows exponentially with respect to the circuit size. Hence the path based SSTA is not easily scalable to handle realistic circuits. On the other hand, the block based SSTA champions the notion of progressive computation. Specifically, by treating every gate/wire as a timing block, the SSTA is performed block by block in the forward direction in the circuit timing graph without looking back to the path history. As such, the computation complexity of block based SSTA would grow linearly with respect to the circuit size. However, to realize the full benefit of block based SSTA, we have to address a challenging issue that timing variables in a circuit could be correlated due to either global variations([4], [5], [6]) or path reconvergence ([7], [8]). Global correlation refers to the statistical correlation among timing variables in the circuit due to global variations such as inter or intra-die spatial correlations, same gate type correlations, temperature or supply voltage fluctuations, etc. Path correlation, on the other hand, is caused by the phenomenon of path reconvergence, that is, timing variables in the circuit can share a common subset of gate/wire blocks along their path histories. Several solutions have been proposed to deal with either of these two types of correlations. In [4], [5], [6], the dependence on global variations is explicitly represented using a canonical timing model. However, these

approaches did not take into account the path correlations. In [8], a method based on common block detection is introduced to deal with the path correlations. However, this method does not address the issue of dependence on global variations. To the best of our knowledge, there is no existing method that has dealt with both types of correlations simultaneously. We present a novel block based SSTA modeling in this paper that is designed to consider both global correlations and path correlations: We develop a model encompassed with numerical computations and tightness probabilities to conditionally approximate the MAX/MIN operator by a linear mixing operator. We extend the commonly used canonical timing model to be able to represent all possible correlations, including the path correlations, between timing variables in the circuit.

III. SSTA PROBLEM FORMULATION

In this section, we will formally define the problem to be solved.

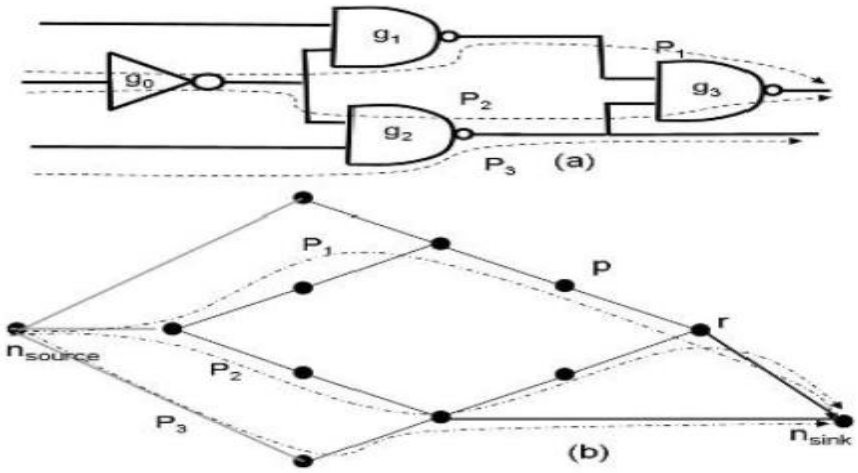

Fig. 2. Combinatorial circuit and its corresponding DAG [9].

Definition: A combinational circuit can be described using a Directed Acyclic Graph (DAG) *G* given as { }, where *N* is the set of nodes corresponding to the input/output pins of the devices in the circuit, *E* is the set of edges connecting these nodes, each with weight , and , are respectively source and sink of the graph. Figure 1(a) shows a digital circuit and its corresponding DAG is shown in Figure 1(b).

Problem Formulation

There are two main challenges in SSTA. The Topological Correlation which emerges from reconvergent paths, these are the ones which originate from a common node and then converge again at another node (reconvergent node). Such correlation complicates the maximum operation as it now has to be computed over correlated RVs. In a circuit example shown in Figure 2, one can see that the two red paths reconverge at the rightmost gate (g3).

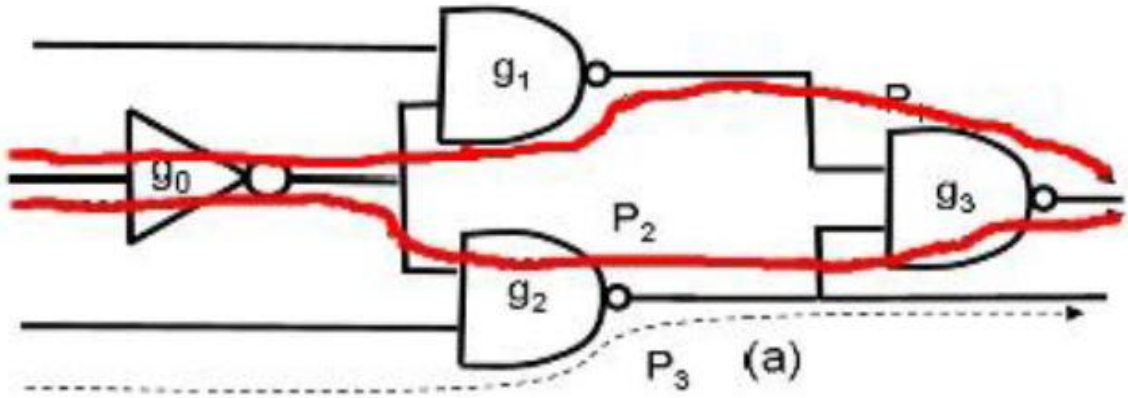

Fig. 3. Topological Correlation [9].

The second challenge is the Spatial Correlation. It arises due to device proximity on the die and gives raise to the problems of modeling delay and arrival time so that correlations are included, as well as preserving and propagating these correlations. Figure 3 shows such two paths correlated by two closely placed gates (g1 and g2).

IV. SOLUTION APPROACHES

The most general and brute force method of solving the above mentioned problem is to use numerical integration [7]. Although exact and applicable, this method is highly computationally expensive and thus, undesired. This leads to another approach, namely, the use of Monte Carlo methods [8]. The exact structure of these methods varies with the problem at hand. However, in general they all follow a common pattern: perform a statistical sampling of the sample space, perform deterministic computation for each sample, and aggregate the results into one final. In order to decrease the error, a lot of samples need to be taken, which, on the other hand, increases the computation effort. Therefore, probabilistic analysis methods are highly desired. Two such exist, one is the *Path-based* approach and the other is the *Block-based* approach. The Path-based approach constructs a set of nodes that are likely to form the critical paths. The delay for each of these paths is then computed and a statistical maximum is performed over these results to yield the worst case delay.

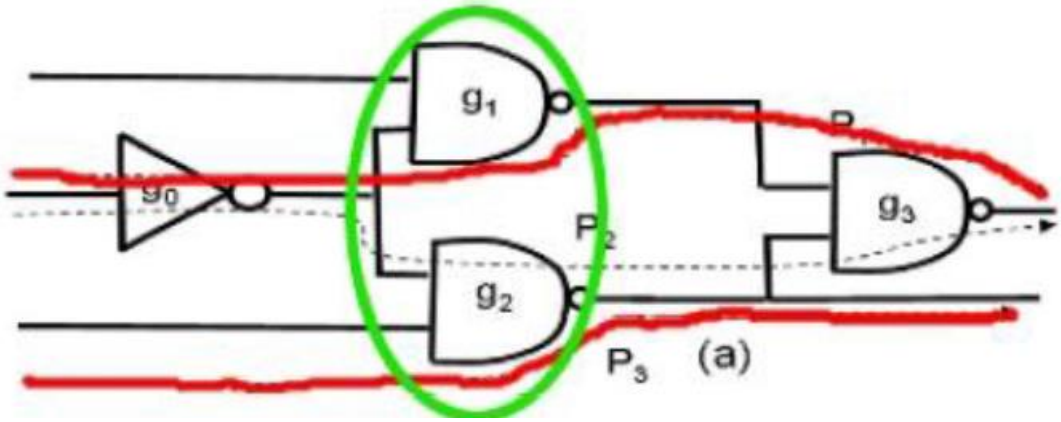

Fig. 4: Spatial Correlation [9]

However, there are several problems associated with this approach. Sometimes it is hard to construct a set of likely critical paths. Therefore, the worst case scenario can be unintentionally omitted. This significantly increases the number of computations needed. Therefore, it is desired to use the Block-based approach. There instead of

constructing critical paths the whole graph is traversed node by node. For all fan-in edges to a node the associated delay is added to the arrival time at the source node (the node upstream of the current one). The final arrival time at the node is computed using a maximum operation over the previous results. This approach has the advantage of propagating only two times, the rise and the fall time.

V. CONCLUSION

In this paper, we have presented the implementation of tightness probability based SSTA on Vector Thread Architecture as well as a GPU GeForce 8800 GTX architecture. Tightness probability based SSTA is computationally expensive, but crucial in design timing closure since it enables an accurate analysis of the delay variations. Our implementation computes multiple timing analysis evaluations for a single gate in parallel. Threads which execute in parallel do not have data or control dependencies on each other. All threads execute identical instructions, but on different data. Our results indicate that our approach can provide 282 times speedup when compared to a conventional CPU implementation.

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